REMARKS

Reconsideration of the above-identified Application is respectfully requested. Claims 1-12 are in the case. Claims 1, 2, 5-7 and 9-11 have been amended. Claims 4, 8 and 12 have been canceled without prejudice, their being considered, upon reflection, directed to consequence rather than structure.

Regarding the rejection of Claims 1-12 under 35 U.S.C. § 112, second paragraph, as allegedly being indefinite, Claims 1, 5 and 9 have been amended to improve the form thereof, and eliminate any alleged indefiniteness. Thus, for example, in Claim 1 it is clear that the control signal generator is connected to the control input of the first multiplexer, and that the clock edge selector circuit in Claims 1 and 9 are connected to respective multiplexers, the clock edge selector circuit of Claim 5 having previously already so recited such connection. It is respectfully submitted that the grounds for this rejection have been overcome, and it is therefore respectfully requested that this rejection be reconsidered and withdrawn.

Regarding the rejection of Claims 1-12 under 35 U.S.C. § 102(e), as allegedly being anticipated by the patent to McCracken et al., Claims 1, 5 and 9 have been amended to overcome the rejection, with Claims 5, 8 and 12 having been canceled, thus rendering the rejection moot with respect thereto. The patent to McCracken et al. apparently relates to a configurable synchronizer for double rate synchronous dynamic random access memory (DDR-SDRAM). Unlike the invention as set forth in the remaining claims under this rejection, the patent to McCracken et al. is concerned with synchronizing DDR-SDRAM. By contrast, the invention as, for example, set forth in Claim 1 is directed to a state machine input/output circuit, an important objective of which is programmability without necessarily having prior knowledge of an application device being controlled. Claim 1 now recites that the memory element recited therein has "a plurality of storage elements, each storage element being adapted to store a bit and provide the bit as an output of said memory." In addition, Claim 1 recites a first multiplexer ... having a plurality of inputs receiving the outputs of said memory...." Similarly, Claim 5 now recites "a

memory having a plurality of storage elements, each storage element being adapted to store a bit and provide the bit at a memory output of said memory, said memory outputs being connected to the inputs of said second multiplexer...." Also similarly, Claim 9 now recites "a memory having a plurality of storage elements, each storage element being capable of storing a bit and providing the bit as an output of said memory...." Thus, in Claims 1, 5 and 9 it is now clear that the bits that are stored in the memory are provided to the inputs of the recited multiplexer. By contrast, the patent to McCracken et al., not being concerned with a programmable state machine input/output circuit, but, rather, being concerned with synchronizing DDR-SDRAM, shows multiplexer 104 receiving a high strobe signal and a low strobe signal at its inputs, for adaptation to, selectably, 4-bit or 8-bit DDR-SDRAM, the output of multiplexer 104 being subsequently used to control synchronization of synchronizers 44. Note that a strobe signal is not provided from a storage element, but, rather, is a timing signal generated during an access cycle.

It is therefore respectfully submitted that Claims 1, 5 and 9 distinguish patentably over the patent to McCracken et al., whether considered by itself or in any combination with any of the other art of record, which is even less relevant than the patent to McCracken et al. Claims 2-4, 6, 7, 10 and 11 all depend from one of Claims 1, 5 and 9, and so are patentable as well for the same reasons, as well as for the additional limitations found therein. Wherefore, reconsideration and withdrawal of this rejection are respectfully requested.

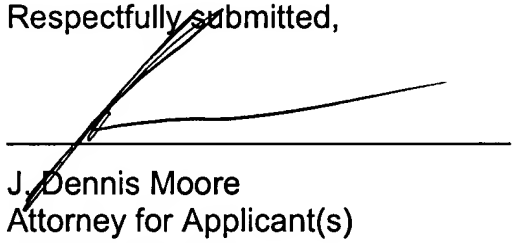
Finally, other amendments of a formal nature have been made to the claims to improve their clarity, in a sincere effort to render the instant application in form for allowance. Thus, to eliminate potential confusion and lack of clarity, all instances of "couple" and words having "couple" as their root have been changed to "connect" and corresponding words having that as their root, to maintain a consistent terminology throughout the claims. Of course, it is understood that when the term "connect", "connected", or the like, is used in the claims, it is understood to mean an electrical connection that may or may not have intervening elements.

It is respectfully submitted that the claims recite the patentably distinguishing features of the invention and that, taken together with the above remarks, the present application is now in proper form for allowance. Reconsideration of the application, as amended, and allowance of the claims are requested at an early date.

While it is believed that the instant amendment places the application in condition for allowance, should the Examiner have any further comments or suggestions, it is respectfully requested that the Examiner contact the undersigned in order to expeditiously resolve any outstanding issues.

To the extent necessary, the Applicants petition for an Extension of Time under 37 C.F.R. §1.136. Please charge any fees in connection with the filing of this paper, including extension of time fees to the Deposit Account No. 20-0668 of Texas Instruments Incorporated.

Respectfully submitted,



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